Notice of Allowability	Application No.	Applicant(s)	
	10/673,677	ZERBE ET AL.	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment dated 4/26/2007*.

2. ☒ The allowed claim(s) is/are *1-17,19-21,23 and 25-55*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-17, 19-21, 23, 25-55 are allowed.

2. The following is an examiner's statement of reasons for allowance:

(1) Regarding claims 1-16:

Claim 1 describes a differential multiple pulse amplitude modulated extractor circuit comprising an upper least significant bit sampler circuit configured to receive a differential multi-PAM input signal and a first differential reference signal, and to generate a first differential sampled output signal; a lower least significant bit sampler circuit configured to receive the differential multi-PAM input signal and a second differential reference signal, and to generate a second differential sampled output signal; and a combiner circuit configured to receive the first differential sampled output signal and the second differential sampled output signal, and to generate a differential LSB output signal indicating an LSB value of the differential multi-PAM input signal. The closest prior art, Zerbe (US 6,396,329 B1) discloses a similar system except a differential multi-PAM input signal, a first differential reference signal and a second differential reference signal. This distinct feature has been added to claim 1, thus rendering claims 1-16 allowable.

(2) Regarding claims 17, 19-21:

Claims 17 and 19 describes a differential multiple pulse amplitude modulated extractor circuit. The closest prior art, Zhang (US 6,614,371 B2) and Jaussi et al (US

6,825,696 B2) disclose a similar circuit except the differential equalization signal has a common-mode similar to the differential multi-PAM input signal. This distinct feature has been added to claims 17 and 19, thus rendering claims 17, 19-21 allowable.

(3) Regarding claims 23 and 25:

Claim 23 describes a differential multiple pulse amplitude modulated extractor circuit. The closest prior art Horan et al. (US 6,462,623 B1) discloses a similar circuit except wherein the differential control signal is applied to the first and second pairs of adjustable resistance elements so as to adjust their resistance value. This distinct feature has been added to claim 23, thus rendering claims 23 and 25 allowable.

(4) Regarding claim 26-30:

Claim 26 describes a differential multi-PAM extractor circuit comprising first and second pairs of adjustable voltage sources connected in series with signal paths for a differential multi-PAM input signal, the first and second pairs of adjustable voltage sources configured to receive a differential control signal; first and second pairs of input transistors, coupled to the first and second pairs of adjustable voltage sources, respectively, and configured to receive voltage adjusted differential multi-PAM input signals from the first and second pairs of adjustable voltage sources, respectively; a load coupled to the plurality of pairs of unbalanced input transistors; and a pair of current sources coupled to the first and second pairs of input transistors, respectively. This distinct circuit renders claims 26-30 allowable.

(5) Regarding claims 31-32:

Claim 31 describes a differential multi-PAM extractor circuit comprising: a differential amplifier circuit configured to receive a differential multi-PAM input signal and to generate an amplified differential multi-PAM signal; a differential automatic gain control circuit, coupled to the differential amplifier circuit, and configured to control gain in the differential amplifier circuit; a first differential sampler circuit, coupled to the differential amplifier circuit and the differential automatic gain control circuit, and configured to sample the amplified differential multi-PAM signal and to generate a first output signal indicating a most significant bit value of the differential multi-PAM input signal; and a second differential sampler circuit, coupled to the differential amplifier circuit and the differential automatic gain control circuit, and configured to sample the amplified differential multi-PAM signal and to generate a second output signal indicating a least significant bit value of the differential multi-PAM input signal. This distinct circuit renders claims 31-32 allowable.

(6) Regarding claims 33-34:

Claim 33 describes a differential multi-PAM extractor circuit comprising: a first differential amplifier circuit configured to receive a differential multi-PAM input signal and to generate a first amplified differential multi-PAM signal; a second differential amplifier circuit configured to receive the differential multi-PAM input signal and to generate a second amplified differential multi-PAM signal; a first differential automatic gain control circuit, coupled to the first differential amplifier circuit, and configured to control gain in the first differential amplifier circuit; a second differential automatic gain control circuit, coupled to the second differential amplifier circuit, and configured to

control gain in the second differential amplifier circuit; a first differential sampler circuit, coupled to the first differential amplifier circuit and the first differential automatic gain control circuit, and configured to sample the first amplified differential multi-PAM signal and to generate a first output signal indicating a most significant bit value of the differential multi-PAM input signal; and a second differential sampler circuit, coupled to the second differential amplifier circuit and the second differential automatic gain control circuit, and configured to sample the second amplified differential multi-PAM signal and to generate a second output signal indicating a least significant bit value of the differential multi-PAM input signal. This distinct circuit renders claims 33-34 allowable.

(7) Regarding claims 35-36:

Claim 35 describes a differential multi-PAM extractor circuit comprising: a first differential amplifier circuit configured to receive a differential multi-PAM input signal and to generate a first amplified differential multi-PAM signal; a second differential amplifier circuit configured to receive the differential multi-PAM input signal and to generate a second amplified differential multi-PAM signal; a differential automatic gain control circuit, coupled to the first differential amplifier circuit and the second differential amplifier circuit, and configured to control gain in the first differential amplifier circuit and the second differential amplifier circuit based at least in part upon the first amplified differential multi-PAM signal; a first differential sampler circuit, coupled to the first differential amplifier circuit and the differential automatic gain control circuit, and configured to sample the first amplified differential multi-PAM signal and to generate a first output signal indicating a most significant bit value of the differential multi-PAM

input signal; and a second differential sampler circuit, coupled to the second differential amplifier circuit, and configured to sample the second amplified differential multi-PAM signal and to generate a second output signal indicating a least significant bit value of the differential multi-PAM input signal. This distinct circuit renders claims 35-36 allowable.

(8) Regarding claim 37-55:

Claim 37 describes a differential multi-PAM extractor circuit comprising: a plurality of differential amplifier circuits configured to receive a differential multi-PAM input signal and to generate a plurality of amplified differential multi-PAM signals; a plurality of adjustable offset voltage sources, coupled to the plurality of differential amplifier circuits, respectively, and configured to provide a plurality of offset voltage signals to the plurality of differential amplifier circuits, respectively; and a plurality of differential multiple-sampler circuits, coupled to the plurality of differential amplifier circuits, respectively, and configured to multiple-sample the plurality of amplified differential multi-PAM signals, respectively, to generate a plurality of multiple-sampled multi-PAM signals, respectively, and to determine a most significant bit value and a least significant bit value of the differential multi-PAM input signal. This distinct circuit renders claims 37-55 allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M Lee
Examiner
Art Unit 2611
7/18/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER